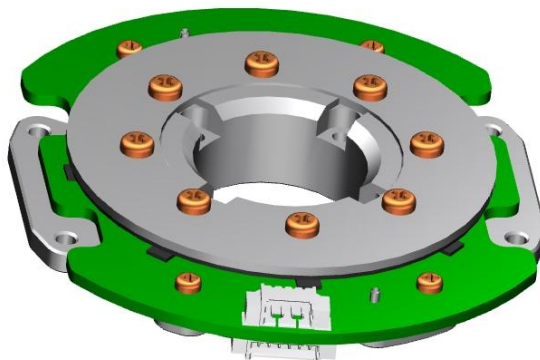


Magnetic linear position encoder

Product series: EAS-009

Product part number: EAS-009-A

Version: Ver1.0.1



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1. Description

EAS series product is an absolute linear position detection magnetic encoder. The sensor can be used in a movement control system to detect the position, speed of the system.

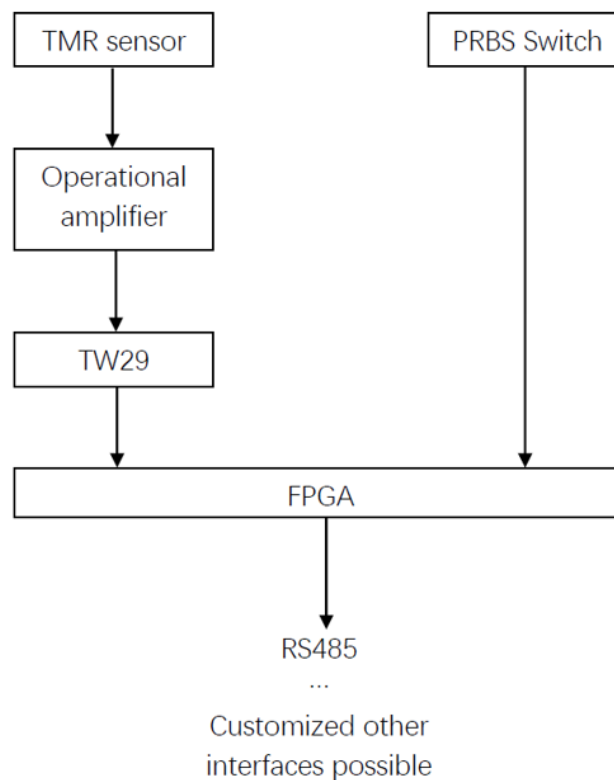
The sensor uses non-contact detection method based on TMR magnetic sensing technology. The magnetic scale has two magnetic tracks (incremental and absolute tracks).

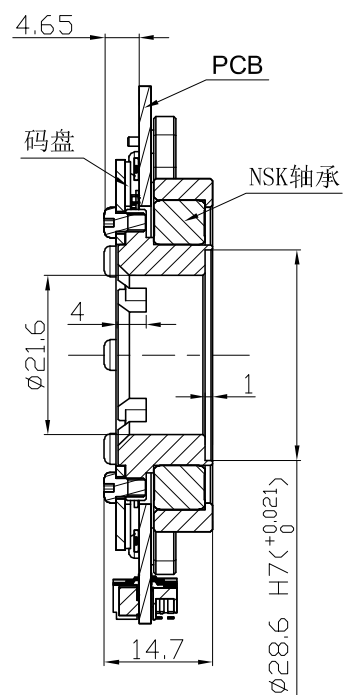
The sensor has build-in signal processing circuit, and a digital output of RS485 format.

EAS series product has the following features:

- True absolute value system
- Absolute position dual track system
- Customized sensor chips
- The system is self-calibrating
- Resolution up to 24 bits
- The repeatability is 3.6 arc seconds
- Absolute positioning accuracy 15~20 arcseconds
- RS485 interface

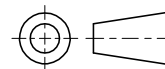
2. Product part number



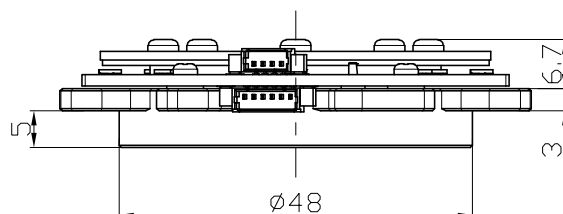


SECTION A-A

1	VCC
2	GND
3	A+
4	B-



插座: A1250WR-S-04PDO1
插头: A1250H-04PNOWNPNOOG
插头端子: A1250-GPE-A
厂家: 灿达电子工业股份有限公司



4. Electrical characteristic

4.1 Electrical connection

Lead	NAME
1	VCC
2	GND
3	A+
4	B-

4.2 General parameter

Operating and storage temperature	-40°C to $+105^{\circ}\text{C}$ (Note: The operating temperature of the diode on the encoder is -40°C to $+85^{\circ}\text{C}$)
Humidity	70%Rh
External magnetic field (thickness direction)	± 100 mT
Shock (dependent on installation)	100 g
Vibration (dependent on installation)	80

4.3 Environmental parameter

Supply voltage	4.75V~5.25V
Current	100 mA~150 mA
Connector	4-pin
Start-up time	100 ms
ESD (HBM)	HBM, Class 2, ± 2 kV

4.4 System parameter

Parameter	Unit	Min	Typ	Max	Comment
Resolution	bit		12		
Maximum speed	RPM		10000		EAS-009-A
			1000		EAS-009-B
Repeatability	arcsec			± 3.6	Bidirectional 3 cycles
Absolute position error	arcsec	± 15		± 20	
Input bandwidth	kHz			2	
Noise	$^{\circ}$		± 0.0005		

5.1 RS485 protocol interface

5.1 Summarize

Item	Description	Remark
Transmission type	Differential drive	RS485
Receiving type	Differential drive	RS485
Transmission data	Single turn data	24bits
Communication rate	2.5Mbps	

5.2 Communication interface

Communication parameter	
Baud rate	2.5M
Baud rate	8bits
Parity check	NC
Stop bit	1
Flow control	NC
Request communication mode	Passive corresponding communication

5.3 Frame format

Request	Control field													
	CM													
Transmission data from		<5 μ s	Control	Status	Data field								CRC field	
			CM	SA	D0	D1	D2	D3	D4	D5	D6	D7	CRC	

5.4 Details

5.4.1 Control field (CM)

The following table shows the structure of the control domain.

Start bit	Sink code			Data ID code				ID parity	Delimiter
0	0	1	0	dc0	dc1	dc2	dc3	dc4	1

(1) Start bit: fixed.

- (2) Sink code: Fixed.
(3) Data ID code: See Table 6-4-1.
(4) ID parity: This is the parity of the data ID code.
(5) Separator: fixed.

Table 5-4-1 Data ID code table

Application	Data ID	Code				Parity
		dc0	dc1	dc2	dc3	dc4
Readout of data	Data ID 0 (0x02)	0	0	0	0	0
	Data ID 1 (0x8A)	1	0	0	0	1
	Data ID 2 (0x92)	0	1	0	0	1
	Data ID 3 (0x1A)	1	1	0	0	0
Writing to EEPROM	Data ID 6 (0x32)	0	1	1	0	0
Readout from EEPROM	Data ID D (0xEA)	1	0	1	1	1
Reset	Data ID 8 (0xC2)	0	0	0	1	1
	Data ID C (0x62)	0	0	1	1	0

5.4.2 State Area (SA)

The state domain structure is shown in Table 5-4-2.

Table 5-4-2 state domain structure

Start bit	Information				Encoder error		Communication alarm		Delimiter
0	sd0	sd1	sd2	sd3	er0	er1	cl0	cl1	1

- (1) Start bit: fixed.
(2) Information: All fixed as "0".
(3) Encoder error: sends logic "1" when any error occurs in the encoder.

5.4.3 Data field

The relationship between data ID codes and data fields is shown in Table 5-4-3.

Table 5-4-3 Lists the data domains

Data ID code	D0	D1	D2	D3	D4	D5	D6	D7
Data ID 0 (0x02)	AS0	AS1	AS2					

Note: The blank in the table above indicates the number not transmitted

5.4.4 CRC Verification Domain (CRC)

Table 5-4-4 shows the CRC domain structure.

Table 5-4-4 CRC domain structure

Start bit	CRC code(LSB first)								Delimiter
0	cr0	cr1	cr2	cr3	cr4	cr5	cr6	cr7	1

(1) Start bit: fixed.

(2) CRC check code: This code conforms to the equation $G(X) = X^8 + 1$ ($X = cr0 \sim cr7$). The data is first arranged by LSB. The code is calculated based on all bits of all fields except CRC fields, excluding the start bit and separator.

(3) Separator: fixed.

5.4.5 Structure of Detailed status bits

Detailed status	
bit12	flash_crc_error
bit13	magic_error
bit14	temp_alarm
bit15	chip_fflt
bit16	prbs_error

5.4.6 Transmit and receive interface circuit diagram

An example of the transmit and receive interface circuit diagram is shown in Figure 5-4-5.

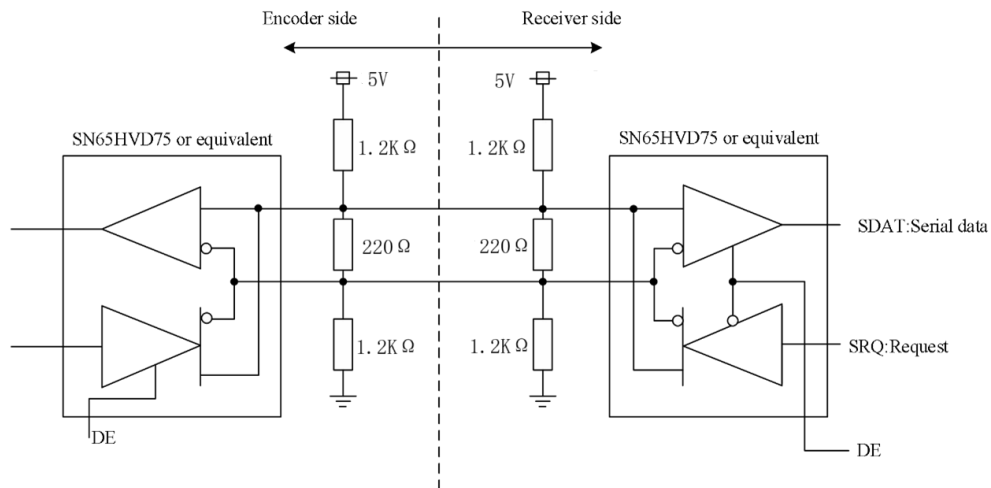


Figure 5-4-5 Example of transmit and receive interface circuits

When the encoder transmits data, do not send any requests to the encoder. If any requests are sent to the encoder in error during this period, the encoder's interface circuit may be interrupted. In addition to transmitting data, the encoder is always in receive mode.

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